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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,799	02/06/2004	Mieno Fumitake	021653-004600US	8454

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EXAMINER	
LEE, CALVIN	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 03/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,799	FUMITAKE et al.	
	Examiner	Art Unit	
	Lee, Calvin	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-19 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 1-6 and 11-16 is/are allowed.

6)☒ Claim(s) 7, 8, 17, and 18 is/are rejected.

7)☒ Claim(s) 9, 10, and 19 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 12 July 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4/26/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

OFFICE ACTION

Specification

1. The specification is objected to because of the following informality:

Page 3, line 14, replace "which ahs a cell" with --which has a cell--

Page 4, line 26, replace "0.13 microns and less" with --0.13 microns or less--

Claim Objections

2. Claims 9, 10, and 19 are objected to because of the following informality:

Claim 9, line 2, claim 10, line 3, and claim 19, line 4, replace "and less" with --or less--

Drawings

3. Figure 9 is objected to as failing to comply with 37 CFR 1.84(p)(5) because it includes the reference character (903) not mentioned in the description [see page 9].

Claim Rejections - 35 U.S.C. § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-10 are rejected under 35 U.S.C. 102(**b**) as anticipated by *Cho et al.*

Cho et al (US 6,242,332) discloses a method for forming a self aligned contact region for a dynamic random access memory device, comprising the steps of:

-providing a semiconductor substrate **100a** having a cell region with its bit line regions and capacitor contact regions [Fig. 3B]

-forming in the cell region first, second, third, and fourth gate structures (having their tungsten silicide layers and overlying caps) [Fig. 3C and col. 5], the second gate structure being spaced by a bit line region to the third gate structure, the first gate structure being spaced by a first capacitor contact region to the second gate structure, the third gate structure being spaced by a second capacitor contact region to the fourth gate structure, wherein the first through fourth gate structures **130a** are characterized by a design dimension of 0.1 micron or less [col. 5, ln.66]

-forming a conformal dielectric layer **118** of silicon nitride overlying the first through fourth gate structures, the bit line region, the first and second capacitor contact regions

-forming an interlayer dielectric material **120** overlying the conformal dielectric layer [Fig. 3E]
-planarizing the interlayer dielectric material by chemical mechanical polishing [col. 6, ln.26]
-forming a masking layer **121** overlying the planarized interlayer dielectric material [Fig. 5A]
-exposing a continuous common region within a portion of the planarized interlayer dielectric material overlying the first through fourth gate structures, the bit line region, the first and capacitor contact regions while maintaining the planarized interlayer dielectric material overlying the gate structure in the peripheral region [Fig. 5C]
-performing a CMP process to remove the exposed portion of the planarized interlayer dielectric layer **120** in the continuous common region to expose the bit line contact, the first and capacitor contact regions while using portions of the conformal layer **118** as a mask to prevent any conductive portions of the first through fourth gate structures from being exposed [Fig. 6A]
-depositing a poly-Si fill material **122** within the continuous common region and overlying the bit line region, the first and second capacitor regions, the first through fourth gate structures to a predetermined thickness [Fig. 6B and col. 7, ln.65]
-planarizing the poly-Si fill material to reduce the predetermined thickness and to simultaneously reduce a thickness of a portion of the interlayer dielectric material **120** to a vicinity of an upper region of the first through fourth gate structures
-continuing the planarization of the poly-Si fill material and the interlayer dielectric material to expose portions of the first through fourth gate structures while leaving portions of the poly-Si fill material on the bit line region, and the first and second capacitor contact regions [Fig. 6C], so as the poly-Si fill material on the first capacitor contact region is isolated from the poly-Si fill material on the bit line region and the poly-Si fill material on the second capacitor contact region is isolated from the poly-Si fill material on the bit line region [col. 8].

Claim Rejections - 35 U.S.C. § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 11-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Cho et al* in view of *Jin et al (US 6,576,963)*.

Cho et al is silent about a peripheral region. *Jin et al* discloses "a method of forming self-aligned contact holes is applied only to a cell area but may be applied to a peripheral circuit area" [col. 2, ln.20]. It would have been obvious to one having ordinary skill in the art to have modified the method of *Cho et al* by utilizing a contact formation on a peripheral region also if the integration density is increased.

Contact Information

8. Any inquiry concerning this communication from the Examiner should be directed to *Calvin Lee* at (571) 272-1896 from 7:00AM to 5:00PM (Monday-Thursday, Eastern Time). If attempts to reach the examiner by telephone are unsuccessful, Art Unit 2825's Supervisory Patent Examiner *David C. Nelms* can be reached at (571) 272-1787.

Any inquiry relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0596. The central fax number is (703) 872-9306 for all communications to be entered (e.g., amendments, remarks, IDS, etc.)

David Nelms
Supervisory Patent Examiner
Technology Center 2800

February 8, 2005